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APPLICATION NOTE

Introducing the MCS® 251 Microcontroller—the 8XC251SB

YONG-YAP SOH
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Introducing the MCS® 251 Microcontroller—8XC251SB

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INTRODUCTION

The MCS® 251 microcontroller is Intel's next generation MCS 51 microcontroller. The first product in the MCS 251 architecture, the 8XC251SB, is binary code and pin compatible with current 8XC51FX microcontrollers. Utilizing an instruction pipeline and a register-based architecture, the 8XC251SB CPU can execute some instructions in the shortest time of one state compared with six states in the 8XC51FX. The instruction set is also enriched with 16-bit and 32-bit capability.

The 8XC251SB has a larger and more flexible memory space. The memory is now linearly addressed through its internal 24-bit and external 17-bit addressing capability. A hardware watchdog timer is also implemented in the 8XC251SB to provide more reliable system designs. As such, the 8XC251SB provides an easy, low-cost, low-risk, and yet high-performance and reliable upgrade path for the MCS 51 microcontrollers.

This Applications Note assumes that readers are familiar with MCS 51 microcontrollers. It gives an overview of the 8XC251SB, highlights the 8XC251SB's new features, and describes the compatibility of the 8XC251SB and 8XC51FX as well as their differences.

For more detailed understanding of the 8XC251SB, please refer to the *8XC251SB User's Manual*, datasheets or other applications notes (see "Additional References").

8XC251SB FEATURE OVERVIEW

The 8XC251SB is a fully static design. It operates at frequencies as low as 0 Hz. The first product is initially available with maximum frequencies of 12 MHz and 16 MHz. The operating voltage is from 4.5V to 5.5V. It is initially available in a 44ld PLCC package at commercial temperature, namely from 0oC to 70oC.

Other basic features of 8XC251SB are:

- Instruction pipeline and register-based architecture
- Linear addressing
- 16-Kbyte on-chip OTPROM/ROM (optional)
- 128-Kbyte external code/data memory space
- 1-Kbyte on-chip data RAM
- 64-Kbyte extended stack space
- Configurable for page mode, external wait state and 17th-bit address
- Enriched instruction set
- 3 16-bit timer/counters
- 1 serial port
- 5 PCA modules
- 1 hardware watchdog timer

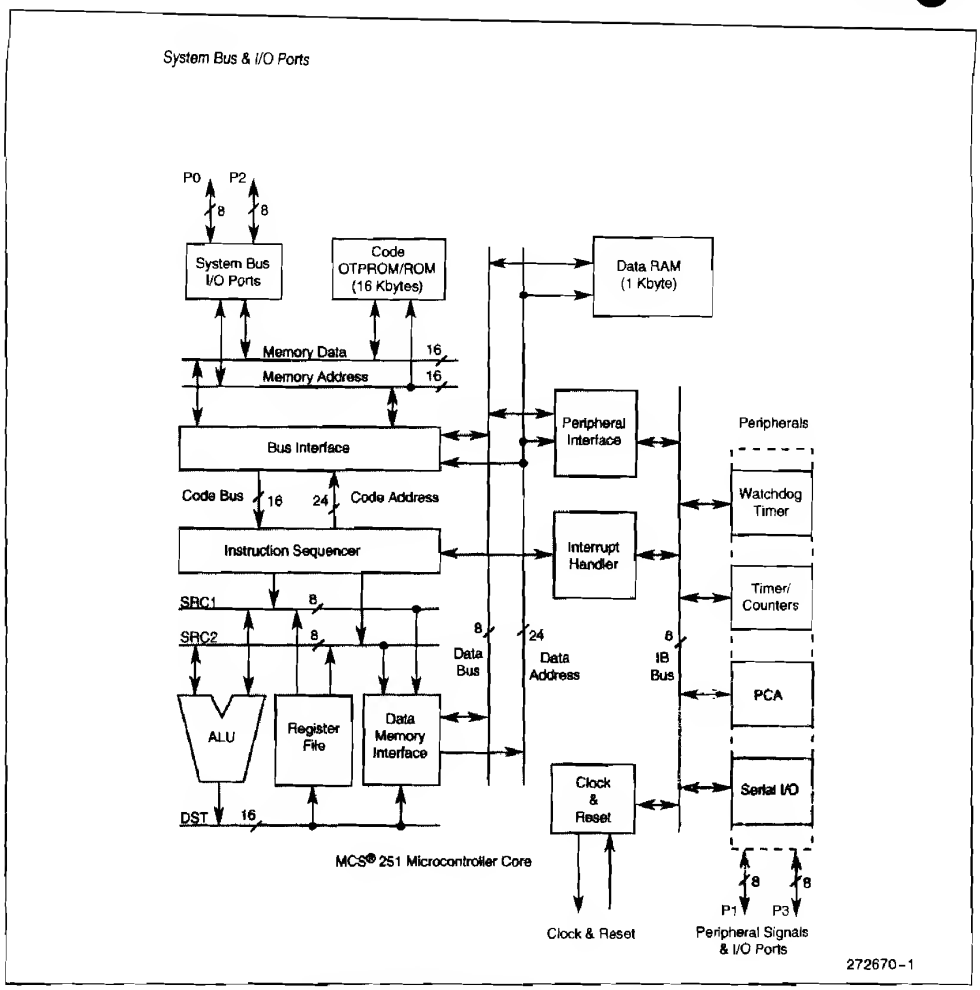

Figure 1. 8XC251SB Functional Block Diagram

CPU ARCHITECTURE

The 8XC251SB CPU is designed with an instruction pipeline architecture. With the pipeline full, some instructions can be executed in the shortest time of one state (or two oscillator clocks) running from internal program memory and two states running from external program memory. Compared with the shortest time of six states per machine cycle for the 8XC51FX, the instruction throughput time for the 8XC251SB has been improved significantly.

The 8XC251SB CPU is also designed with a register-based architecture. A 40-byte general purpose register file, capable of byte, word or double-word register addressing, can also be used for register to register operations.

For example, in the 8XC251SB, the user can move a byte between registers with just one instruction (Example 1). In the 8XC51FX, which has an accumulator-based architecture, two instructions are needed to achieve the same result (Example 2).

Example 1:

```
MOV R7, R0      ; 1 instruction, 1 state
                ; (in source mode) for
                ; 8XC251SB
```

Example 2:

```
MOV A, R0       ; 2 instructions,
                ; 12 states for 8XC51FX
MOV R7, A
```

MEMORY ORGANIZATION

The 8XC251SB has 24-bit address lines internally. As such, it has 16 Mbytes of memory space addressing capability. However, only four 64-Kbyte regions of memory are available for use in the 8XC251SB. These four regions of memory are 00:, 01:, FE: and FF:. The *region* here denotes upper byte of the 24-bit address.

Program Counter and Data Pointer

The 8XC251SB has a 24-bit program counter and a 24-bit data pointer. The 24-bit program counter is always initialized to FF0000H, the starting address for program execution. In an 8XC51FX-compatible configuration, the upper byte of the program counter is transparent to the user.

The upper byte of the 24-bit extended data pointer is initialized to 01H. If the 8XC251SB is configured for use in an 8XC51FX-compatible system, this upper byte is transparent to the user, who works with the 16-bit data pointer, DPTR. The data pointer is located in both register file and special function registers (SFRs).

Program Memory and External Data Memory

The 8XC251SB has a linear addressing architecture. As such, both program and external data memories can be mapped separately into a 128-Kbyte memory space. However, the 8XC51FX has both program and external data memories overlapped in one 64-Kbyte memory space.

By default, the program memory for 8XC251SB is initialized and mapped into region FF:, while the external data memory for 8XC251SB is initialized and mapped into region 01: (Figure 2). The program memory space includes the optional 16-Kbyte internal ROM or OTPROM.

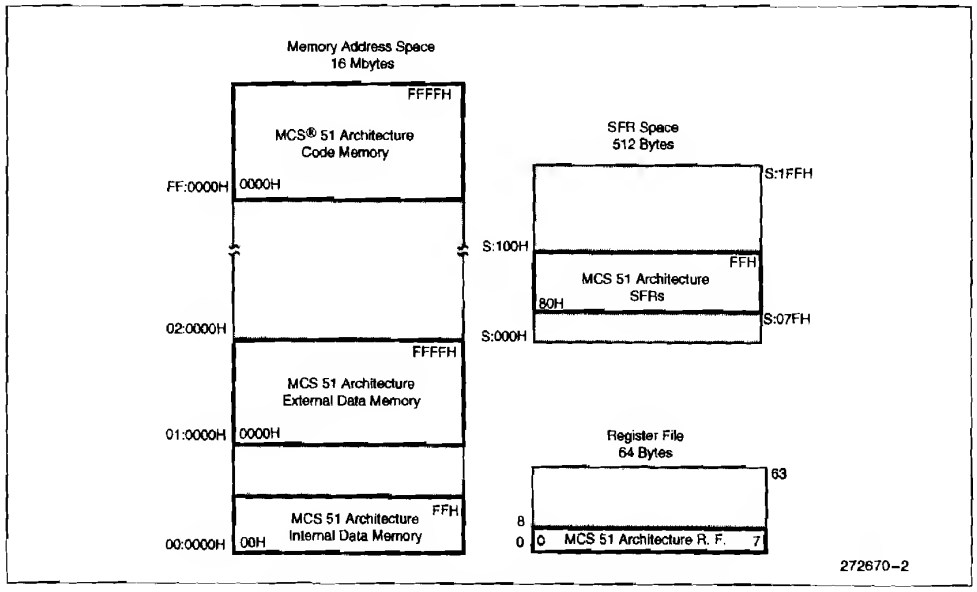

Figure 2. MCS® 51 Memory Mapping in 8XC251SB

Program and external data memories can be mapped into any other regions as well. However, the program memory cannot be mapped into region 00: where the general purpose registers R0-R7 and the on-chip data RAM occupy. The program code cannot be loaded into and execute from the on-chip data RAM as well.

For compatibility with the 8XC51FX, only 16 address lines are used in the 8XC251SB to access external memory. To differentiate the external program and external data memories access, separate control pins are used as in the 8XC51FX. These control pins assert RD# and WR# signals for external data memory reads and writes, and PSEN# signal for external program memory fetches.

Special Function Registers (SFRs)

The 8XC251SB has a separate 128-byte SFR space with addresses S:0080H to S:00FFH (Figure 2). All the SFRs are bit-addressable. The only bit-addressable SFRs of the 8XC51FX are those with addresses of the form X0H and X8H.

Internal Data Memory

The 8XC251SB internal data memory is mapped at region 00: of memory.

Thirty-two bytes registers at locations 00:0000H to 00:001FH are divided into four banks, each having eight general purpose registers R0-R7. One Kbyte of on-chip data RAM is located from 00:0020H to 00:041FH. Of the one Kbyte of RAM, 96 bytes are bit addressable. The bit-addressable memory is located from 00:0020H to 00:007FH (Figure 3).

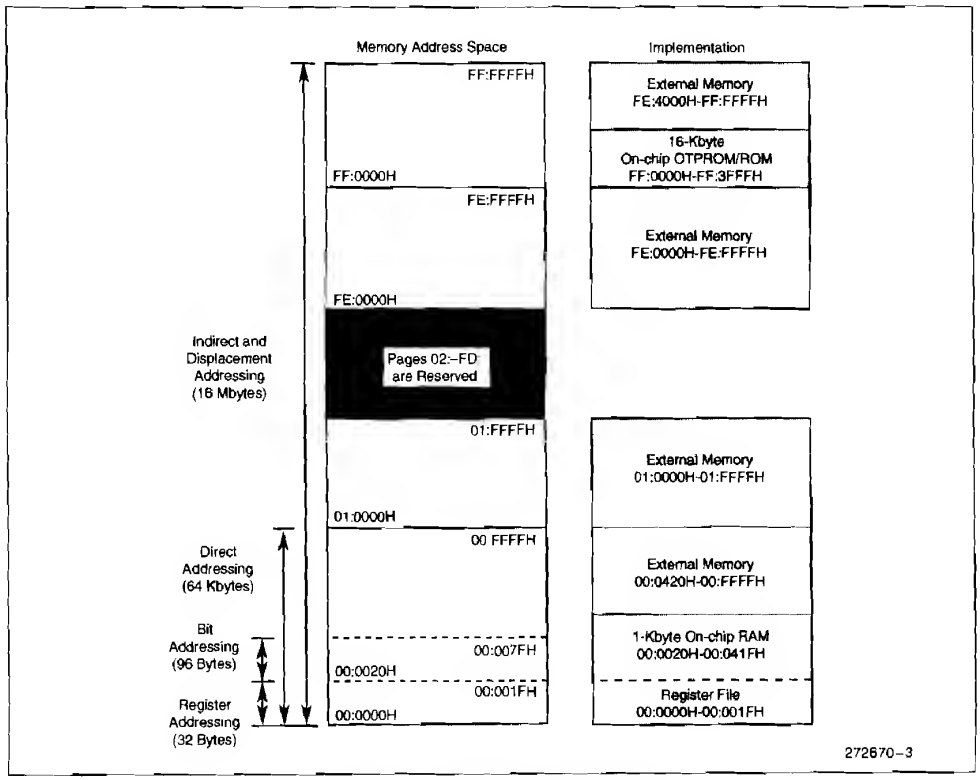

Figure 3. 8XC251SB Memory Mapping

The 8XC51FX has only 256 bytes of on-chip data RAM. Of the 256 bytes of RAM, 32 bytes are used as four banks general purpose registers R0-R7 and 16 bytes are bit addressable. The four banks general purpose registers are located from 00H to 1FH and the bit-addressable memory are located from 20H to 2FH.

Stack Memory and Stack Pointer

The 8XC251SB has 64 Kbytes memory space in region 00: available for use as data memory. The external memory space starting from 00:0420H to 00:FFFFH can be used as an extended stack data memory to the on-chip 1-Kbyte data RAM. The extended stack memory is required for more efficient high-level language programming.

The stack pointer, located in the register file as well as in the SFRs, is initialized to point to location 00:0007H as in the 8XC51FX.

Addressing Modes

The internal data memory addressing for the 8XC251SB is slightly different from the 8XC51FX. The entire 8XC251SB internal data memory space from 00:0000H to 00:FFFFH can be accessed by either direct or indirect addressing (Figure 3). However, the 8XC51FX has only 256 bytes on-chip RAM. The upper 128 bytes of the 8XC51FX internal data memory from 80H to FFH can only be accessed by indirect addressing.

The other regions of memory, namely 01:, FE: and FF: can only be accessed by indirect or displacement addressing. The 8XC251SB SFRs space can only be accessed by direct addressing as in the 8XC51FX.

Register File

The 8XC251SB has a register file. The register file contains 40 bytes of general-purpose registers. These registers include 8 bytes from R0 to R7, 24 bytes from R8 to R31, and 8 bytes from R56 to R63 (Figure 4). The 8XC51FX does not have a register file; it has only four banks of general-purpose registers, each bank comprising eight bytes, R0 to R7.

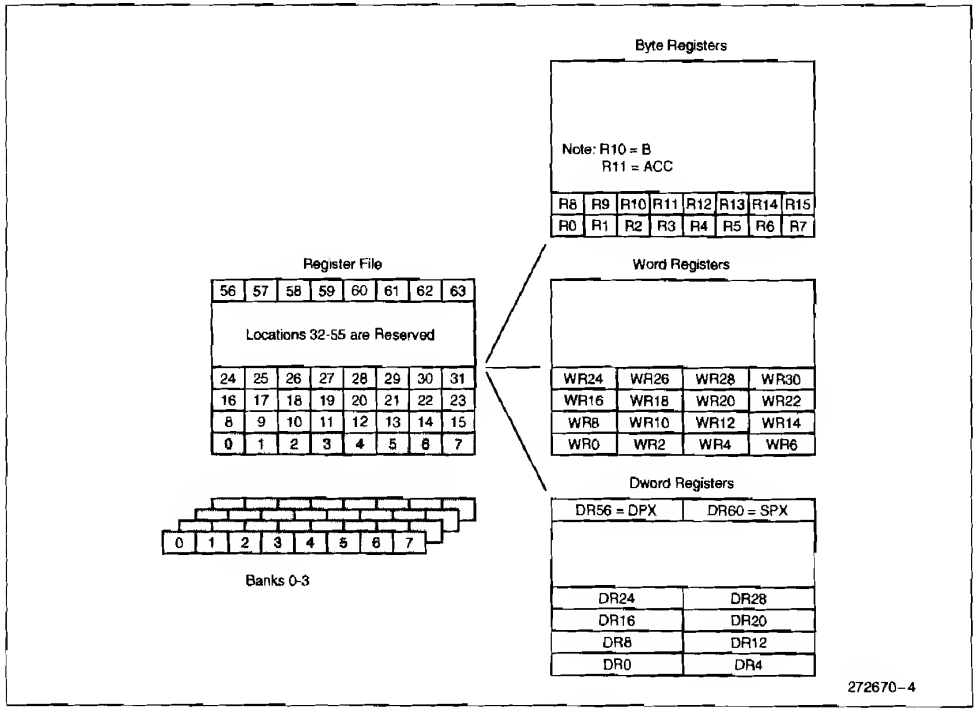

Figure 4. 8XC251SB Register File

To be compatible with the 8XC51FX, registers R0 to R7 are mapped to the internal data memory space as well as the register file, while the remaining 32 registers are located in the 8XC251SB CPU. The 32 bytes registers in the CPU provide flexible and powerful register-to-register operations as well as register addressing.

128 Kbytes Memory Space

The RD# pin of the 8XC251SB can also be configured as address pin A16. With this configuration, two of the 64-Kbytes blocks of memories can be used as contiguous 128 Kbytes memory space. These two blocks of memory can be used as program memory, external data memory, or a mixture of both.

In this configuration, the PSEN# signal is used to strobe the outputs of the entire 128 Kbytes of memory. Register addressing through a double-word register from the register file activates the PSEN# signal for accessing the entire 128 Kbytes memory space. Example 3 illustrates moving a data byte in R4 to one of the 128 Kbytes of memory addresses contained in the double-word register DR56.

Example 3:

```
MOV @DR56, R4      ; Move data in
                   ; 128 Kbytes memory
                   ; space for 8XC251SB
```

CONFIGURATION

The 8XC251SB has two configuration bytes, which do not exist in the 8XC51FX. By programming the configuration bytes, the 8XC251SB can be configured to have the following features:

- Binary mode
- External wait states
- Extended ALE
- Page mode
- OTPROM/ROM memory mapping mode
- RD# Disable/A16 Enable Modes
- MCS® 51 Interrupt Mode

Binary Mode

The 8XC251SB provides binary code compatibility through the binary mode. In binary mode, the 8XC251SB is able to run MCS 51 microcontrollers' binary codes without recompilation. However, the maximum power and highest performance of 8XC251SB can be obtained when binary mode is off (ie. source mode).

External Wait States/Extended ALE

The 8XC251SB provides the flexibility to interface with slow and fast memories. When a slow external memory interface is needed, one wait state can be added to the PSEN#, RD# and WR# signals. The ALE signal can be extended for an additional state as well to further slow down the external memory interface.

Page Mode

For a fast external program memory interface, the data bus can be swapped from port 0 to port 2 in page mode. The data byte is then time-multiplexed with the upper address byte on port 2.

In page mode, if successive code fetches are to the same 256-byte block of memory, the ALE signal latches the upper address byte only once, which is used for both fetches. Once the upper address byte is latched, Port 2 is available to serve as the data bus, while port 0 carries the lower address byte. Because ALE is not asserted for the second fetch, this fetch takes only one state.

OTPROM/ROM Memory Mapping Mode

The upper 8 Kbytes of on-chip program memory, from FF:2000H to FF:3FFFH can be mapped into the upper 8 Kbytes of region 00: (00:E000H to 00:FFFFH). This memory can be used for look up tables or constant data. This data then shares the lowest 64 Kbytes of memory (region 00:) with on-chip RAM data. Both types of data can then be easily accessed with 16-bit addressing.

RD# Disable/A16 Enable Modes

The RD# pin can be disabled and used as a normal I/O port pin. The RD# pin can also be configured as address pin A16 to access 128 Kbytes of external memory. On both modes, PSEN# is used to strobe for the external memory outputs.

MCS® 51 Interrupt Mode

To maintain backwards compatibility for users who use RET & RETI interchangeably, the MCS 51 Interrupt Mode will restrict the bytes pushed on the stack during an interrupt to the lower two bytes of Program Counter. Otherwise, the 8XC251SB will push three bytes of Program Counter and one byte of new program Status Word, PSW1 into the stack. This mode restricts the code space to the region FF: while using interrupts.

INSTRUCTION SET

In the MCS 51 architecture, the instruction opcode is encoded in one byte of hex code, which provides 256 possible combination of instructions. The MCS 51 microcotroller has implemented a total of 255 instructions. The reserved location, A5H is used for binary code compatibility of MCS 51 microcontroller programs used with MCS 251 microcontrollers.

Binary Code Compatibility

When 8XC251SB is configured in binary mode, it can run both MCS 51 microcontroller instructions as well as new 8XC251SB instructions (Table 1). The new 8XC251SB instructions are encoded with prefix 'A5H' when used in this mode. Running MCS 51 microcontroller instructions alone in the 8XC251SB ensures binary code compatibility with MCS 51 microcontrollers.

In source mode, the MCS 51 microcontroller's instructions using general purpose registers R0-R7 are encoded with prefix "A5H". No prefix "A5H" is encoded for other MCS 51 microcontroller's instructions. Running new 8XC251SB instructions in source mode maximizes the usage of 8XC251SB resources for highest performance.

Table 1. Compatibility of MCS 51 Microcontroller's Instruction Set in 8XC251SB

Microcontroller	MCS 51 Microcontroller's Instruction	8XC251SB Instruction
8XC51FX	[MCS 51 Microcontroller's Opcode]	N/A
8XC251SB in Binary Mode	[MCS 51 Microcontroller's Opcode]	A5[8XC251SB Opcode]
8XC251SB in Source Mode	[MCS 51 Microcontroller's Opcode], A5[MCS 51 Microcontroller's Opcode]	[8XC251SB Opcode]

Code Size

The new 8XC251SB instruction opcodes are encoded with one or more bytes of hex code. The code size grows as additional bytes are needed for addressing such as register addressing (other than R0-R7), displacement addressing and addressing the extended memory space. For example, the instruction MOV R8, #55H is encoded with three bytes in the 8XC251SB (Example 4) but MOV R6, #55H is encoded with only two bytes in the 8XC51FX (Example 5).

Example 4:

```
MOV R8, #55H
; The opcode for this instruction in
; the 8XC251SB is 7E 80 55H
; Where,
;       80H is encoded for this
;       instruction using R8
;       (other than R0-R7)
;       55H is encoded for immediate
;       data #55H
```

Example 5:

```
MOV R6, #55H
; The opcode for this instruction in
; the 8XC51FX is 76 55H
; Where,
;       6H is encoded for this
;       instruction using R6
;       55H is encoded for immediate
;       data #55H
```

16-Bit and 32-Bit Capability

The new 8XC251SB instruction set is enriched with 16-bit and 32-bit capability. This helps to reduce the number of instructions used and CPU time consumed. Note that the big-endian architecture of the 8XC251SB has the high-byte in the lower address and the low-byte in the upper address. For example, the word register WR0 consists of R0 and R1, where R0 contains the high byte and R1 contains the low byte (Example 6).

Example 6:

```
MOV WR0, #01ABH
; Where,
;       WR0 = [R0, R1]
;       R0 = #01H, high-byte
;       in the lower address
;       R1 = #ABH, low-byte
;       in the higher address
```

Instruction Timing

With the instruction pipeline architecture, the 8XC251SB instruction execution timing is slightly more complex. When the pipeline is full, the internal bus timing and external bus timing is described as follows.

The fastest internal bus cycles require only one state. The fastest external instruction read cycles and data read cycles require two states. The fastest external write cycles requires 3 states. Instructions that access the I/O ports may require additional states, depending on type of instruction.

PERIPHERALS

The 8XC251SB has the following peripherals:

- 3 16-bit Timer/Counters
- 1 Serial Port, and
- 5 Programmable Counter Array (PCA) Modules

Functionality & Timing

The 8XC251SB has exactly the same peripherals as the 8XC51FX. The 8XC251SB peripherals are controlled through same SFR's and have the same mode of operations as in the 8XC51FX.

For the same operating frequencies, the 8XC251SB peripherals also operate with the same timing as in the 8XC51FX. The 8XC251SB peripherals complete one cycle in 6 states that is equivalent to one machine cycle for the 8XC51FX.

Timer/Counters

The timers are clocked by one twelfth of the oscillator frequency (Fosc/12) and have four modes of operation. As counters, it can count to the speed of Fosc/24 input from T0, T1 or T2 pins. Timer 2 can also be used as up/down counter, or it can output a 50% duty cycle clock with maximum clock rate of Fosc/4 on T2 pin.

Serial Port

The serial port can either be used as half-duplex synchronous serial communication or full-duplex asynchronous serial communication. In synchronous mode, 8-bit data transmits or receives through RXD pin that is synchronized by clock outputs on TXD pin at a fixed baudrate of Fosc/12.

In asynchronous mode, 8 or 9-bit data with a start bit and a stop bit transmit through TXD pin and receive through RXD pin asynchronously. The baudrate of the asynchronous data transmit or receive is variable provided by timer 1 or timer 2 at a maximum baudrate of Fosc/32.

PCA

The PCA has five modules that can be individually programmed as PWM output, high speed output, waveform capture or software timer. The PCA module 4 can also be programmed as software watchdog timer.

HARDWARE WATCHDOG TIMER (WDT)

The 8XC251SB has implemented a hardware WDT in addition to a software WDT configurable from the PCA module 4. The hardware WDT has 14-bit counter, which increments on every 6 states.

The hardware WDT will reset the whole chip when the counter overflows. However, the hardware WDT reset will not drive the reset signal out on RESET pin. The hardware WDT can only be disabled by a reset. This provides a more reliable system design.

The hardware WDT is defaults to disable after an initialization reset. This ensures compatibility with the 8XC51FX. The 8XC51FX does not have a hardware WDT.

I/O PORTS

The 8XC251SB has four 8-bit I/O-ports. The 8XC251SB I/O-ports have same functionality as the 8XC51FX I/O-ports. Port 0 has open-drain structure and port 1 to 3 have weak pull-up structure. The 8XC251SB I/O-ports timing is variable depending on instruction types used.

Alternate Functions

All the 8XC251SB port pins are bi-directional, bit addressable and have alternate functions as in 8XC51FX (Table 2). The alternate functions can only be activated by writing 1's to corresponding port SFR bit latches. Writing 1's to port SFR bit latches also configure them as inputs. The 8XC251SB alternate function has been enhanced with page mode operation and the configurable seventeenth address line.

Page Mode

In page mode, the data byte is coming out from port 2 rather than port 0. The data byte is now multiplexed with the upper address byte, A8-A15. Both port 0 and port 2 drive strong 1's and 0's for address and data output; port 2 floats for data input.

Additional Address Line

The P3.7/RD#/A16 pin can also be configured as address pin A16 to access 128 Kbytes external memory space. The P3.7/RD# pin can also be disabled and used as normal I/O pin.

Table 2. Alternate Functions of the 8XC251SB I/O Pins

Port Pin	Alternate Function
P0.0/AD0- P0.7/AD7	Multiplexed of lower address byte/data for external memory; lower address byte only in page mode
P1.0/T2	Timer 2 external clock input/Programmable clock output
P1.1/T2EX	Timer 2 reload/capture/direction control
P1.2/ECI	PCA external clock input
P1.3/CEX0	PCA module 0 capture input, compare/PWM output
P1.4/CEX	PCA module 1 capture input, compare/PWM output
P1.5/CEX	PCA module 2 capture input, compare/PWM output
P1.6/CEX	PCA module 3 capture input, compare/PWM output
P1.7/CEX	PCA module 4 capture input, compare/PWM output
P2.0/A8- P2.7/A15	Upper address byte for external memory; multiplexed of upper address byte/data in page mode
P3.0/RXD	Serial port input
P3.1/TXD	Serial port output
P3.2/INT0#	External interrupt 0
P3.3/INT1#	External interrupt 1
P3.4/T0	Timer 0 external clock input
P3.5/T1	Timer 1 external clock input
P3.6/WR#	Write strobe for external data memory
P3.7/RD/A16	Read strobe for external data memory; A16

INTERRUPTS

The 8XC251SB provides seven maskable and one TRAP instruction interrupts (Table 3). The maskable interrupts consist of two external interrupts, three timer interrupts, one serial port interrupt and one PCA interrupt. The 8XC251SB interrupts are the same as the 8XC51FX interupts except the priority within level, interrupt timing and the TRAP instruction interrupt.

Priority Within Level

The seven maskable interrupts can be programmed into four different interrupt priority levels. When more than one interrupt requests have the same priority level, they are resolved by hardware interrupt priority within level. Compared with the 8XC51FX, the interrupt priority within level for PCA has been lowered down from 5 to 7, while serial port and timer 2 have been moved up accordingly (Table 3).

Interrupt Timing

The timing of interrupt request, sampling and priority resolution for 8XC251SB has been changed to four states per interrupt cycle compared with six states per machine cycle for 8XC51FX. The interrupt latency for 8XC251SB is estimated from 17 states to the longest of 72 states if DIV instruction is executing while an interrupt request occurs. The 8XC51FX interrupt latency is estimated from 18 states to 54 states.

TRAP Instruction Interrupt

The TRAP instruction when executed will cause an interrupt call that is vectored to address FF:007BH. The TRAP instruction interrupt is always with highest interrupt priority and is intended for use by development tools. The 8XC51FX does not have TRAP instruction.

Table 3. 8XC251SB Interrupts

Interrupt Source	Interrupt Flag	Hardware Clear	Vector Address	Priority Within Level
INT0#	IE0	No (level) Yes (edge)	FF: 0003H	1 (Highest)
Timer 0	TF0	Yes	FF:000BH	2
INT1#	IE1	No (level) Yes (edge)	FF:0013H	3
Timer 1	TF1	Yes	FF:001BH	4
Serial Port	RI, TI	No	FF:0023H	5
Timer 2	TF2, EXF2	No	FF:002BH	6
PCA	CF, CCFn (n = 0-4)	No	FF:0033H	7 (lowest)
TRAP	N/A	N/A	FF:007BH	N/A

ADDITIONAL REFERENCES

The additional and detailed information on the 8XC251SB device functionality and product specifications can be obtained from the following literature:

- *8XC251SB User's Manual* (Order Number 272617)
- *8XC251SB High-Performance CHMOS Single-Chip Microcontroller* datasheet (Order Number 272616)
- AP-709, *Maximizing Performance Using the MCS® 251 Microcontroller—Programming the 8XC251SB* (Order Number 272671)
- AP-710, *Migrating from the MCS 51 Microcontroller to the MCS 251 Microcontroller—Software and Hardware Considerations* (Order Number 272672)

UNITED STATES
Intel Corporation
2200 Mission College Boulevard
P.O. Box 58119
Santa Clara, CA 95052-8119

JAPAN
Intel Japan K.K.
5-6 Tokodai, Tsukuba-shi
Ibaraki, 300-26

FRANCE
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78054 Saint-Quentin-en-Yvelines Cedex

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85622 Feldkirchen/Muenchen

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190 Attwell Drive, Suite 500
Rexdale, Ontario M9W 6H8

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